ABSTRACT OF THE DISCLOSURE

A wafer level chip scale packaging structure and the method of fabricating the same are disclosed to form a sacrificial layer below the bump using a normal semiconductor process. The bump is used to connect the signals between the Si wafer and the PCB. The interface between the sacrificial layer and the PCB is the weakest part in the whole structure. When the stress applied to the bump is overloaded, the interface between the sacrificial layer and the PCB will crash to remove the stress generated by different thermal expansion coefficients of the Si wafer and the PCB. The sacrificial layer would help avoid the crash occurring to the bump to protect the electrical conduction between the Si wafer and the PCB.